What Is Claimed Is:

1. A data processor using a status register and a plurality of register banks to execute instructions,

wherein the status register includes an overflow flag to indicate an overflow of the plurality of register banks.

2. A data processor comprising:

a status register;

a central processing unit including a predetermined register set; and

a plurality of register banks corresponding to the predetermined register set,

wherein the plurality of register banks are used to save storage information held by the predetermined register set when an interrupt occurs, and

wherein the status register includes an overflow flag to indicate an overflow of the plurality of register banks.

3. The data processor according to claim 2,

wherein, when an interrupt exception occurs in a state in which data has been saved

to all banks of the register banks, and

wherein when the accepted interrupt exception is permitted to use the register banks, the central processing unit saves data of the register set to a stack area and reflects an overflow state in the overflow flag.

4. The data processor according to claim 3,

wherein, when the overflow flag indicates an overflow state, if data restoration from the register banks to the register set is directed, the central processing unit restores the data from the stack area to the register set.

5. The data processor according to claim 2,

wherein, when an interrupt exception occurs in a state in which data has been saved to all banks of the register banks, and the accepted interrupt exception is permitted to use the register banks and specified to execute a predetermined exception handling routine, the central processing unit executes the predetermined exception handling routine and does not perform saving to the register banks.

6. The data processor according to claim

1, comprising:

a memory constituting the plurality of register banks; and

a bus dedicated to couple between the memory and a predetermined register set,

wherein the bus includes as many bits as parallel data transfer is allowed in units of plurality of registers contained in the register set.

7. The data processor according to claim 2,

wherein the central processing unit, in response to the occurrence of interrupt exception, saves the status register and a program counter to a stack area, and saves information within the predetermined register set to the register banks.

8. The data processor according to claim 7,

wherein whether to save to the register banks is able to be selected according to factors indicating types of interrupts or priority levels.

9. The data processor according to claim 7, including interrupts to always perform

saving to the register banks and interrupts capable of automatically selecting a stack area as a save location when the number of remaining banks is small.

10. The data processor according to claim 7,

wherein the central processing unit includes in an instruction set a register restore instruction to restore storage information from a register bank last saved to the predetermined register set.

11. The data processor according to claim 10,

wherein, if the register restore instruction is executed when the register banks are empty, predetermined exception service occurs.

12. The data processor according to claim 10,

wherein the instruction set includes a return instruction to restore a value of the program counter and a value of the status register stored in a stack area in interrupt exception handling and enable return to previous program execution processing.

13. A data processor that uses a predetermined register set and a plurality of register banks to execute instructions,

wherein the plurality of register banks are used to save storage information held by the predetermined register set, and

wherein an instruction set of the data processor includes a register restore instruction to restore storage information from a register bank last saved to the predetermined register set, and a return instruction to restore a value of a program counter and a value of a status register saved to a stack area in interrupt exception handling and cause return to previous program execution processing.

14. A data processor including a predetermined register set and a plurality of register banks corresponding to the predetermined register set,

wherein the plurality of register banks are used to save storage information held by the predetermined register set, and

wherein an instruction set of the central processing unit separately includes a register restore instruction to restore storage

information from a register bank last saved to the predetermined register set, and a return instruction to restore a value of a program counter and a value of a status register saved to a stack area in interrupt exception handling and cause return to previous program execution processing.

15. The data processor according to claim 14,

wherein, in task switching using the interrupt exception handling, in return from interrupt exception handling, the register restore instruction is executed to restore data of a register bank in a task of a switching source to the register set,

wherein the restored data is stored in an OS internal table managed by an OS,

wherein register set data of a task of a switching destination is restored from the OS internal table to the predetermined register set, and

wherein the return instruction is executed to transfer control to program execution processing of the task of the switching destination.